In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of exporting emulation information from a data processor integrated circuit, comprising:

collecting internal emulation information from a data processor at a data processor clock rate;

arranging the collected emulation information into a plurality of first information blocks having a first fixed size;

receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks having a second fixed size which differs from the first fixed size of the first information blocks; and

outputting a sequence of the second information blocks from the data processor integrated circuit via a plurality of terminals at a transmission clock rate, said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

2. (Previously Presented) The method of Claim 1, wherein the second fixed size is smaller in size than the first fixed size.

3. (Original) The method of Claim 1, including receiving the sequence of second information blocks externally of the data processor, and re-arranging the emulation information contained in the second information blocks into a plurality of the first information blocks.

4. (Original) The method of Claim 1, wherein each of the first and second information blocks is a packet of emulation information.

5 to 15. (Cancelled)

16. (Previously Presented) An integrated circuit, comprising:

a data processor for performing data processing operations;

a collector coupled to said data processor for collecting emulation information from said data processor at a data processor clock rate and arranging said emulation information into a plurality of first information blocks having a first fixed size;

an exporter coupled to said collector for receiving therefrom said plurality of first information blocks and arranging said emulation information contained therein into a plurality of second information blocks having a second fixed size which differs from the first fixed size of said first information blocks;

a plurality of terminals for outputting information; and

said exporter coupled to said terminals for outputting a sequence of the second information blocks via said terminals at a transmission clock rate, said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

17. (Previously Amended) The integrated circuit of Claim 16, wherein said second fixed size is smaller in size than said first fixed size.

Claims 18 to 26. (Canceled)

27. (Previously Presented) A data processing system, comprising:

an integrated circuit, including a data processor for performing data processing operations;

an emulation controller coupled to said integrated circuit for controlling emulation operations of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing emulation information about said data processing operations, said apparatus including a collector coupled to said data processor for collecting said emulation information from said data processor at a data processor clock rate and arranging said emulation information into a plurality of first information blocks having a first fixed size, and an exporter coupled to said collector for receiving plurality of first information blocks and arranging said emulation information contained therein into a plurality of second information blocks having a second fixed size which differs from the first fixed size of said first information blocks; and

said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, said exporter coupled to said terminals for outputting a sequence of said second information blocks to said emulation controller via said terminals at a transmission clock rate, said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

28. (Original) The system of Claim 27, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

29. (Original) The system of Claim 28, wherein said man/machine interface includes one of a visual interface and a tactile interface.

30. (Previously Presented) The method of Claim 2, wherein:

said first fixed size is an integral multiple of said second fixed size; and

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks includes the steps of

(a) storing a current first information block in a current packet register,

(b) sequentially selecting groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a first bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until all bits of the current packet register are selected,

(c) thereafter storing a next first information block in the current packet register and repeating steps (a), (b) and (c).

31. (Previously Presented) The method of Claim 2, wherein:

said first fixed size is not an integral multiple of said second fixed size; and

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks includes the steps of

(a) storing a current first information block in a current packet register,

(b) sequentially selecting groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number,

(c) storing the current first information block in a last packet register,

(d) storing a next first information block in the current packet register,

(e) selecting a group of the second fixed size bits from a set of bits remaining in the last packet register and bits starting at a first bit of the current packet register, and

(f) thereafter repeating steps (b), (c), (d) and (e).

32. (Previously Presented) The integrated circuit of claim 17, wherein:

said first fixed size is an integral multiple of said second fixed size; and

said exporter includes

a current packet register, and

a combiner connected to said current packet register and said terminals, said combiner operable to

(a) store a current first information block in a current packet register,

(b) sequentially select groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a first bit of said current packet register, subsequent selected groups beginning at a bit following a last bit

of a prior group, until all bits of the current packet register are selected,

(c) thereafter store a next first information block in the current packet register and repeat steps (a), (b) and (c).

33. (Previously Presented) The integrated circuit of claim 17, wherein:

said first fixed size is not an integral multiple of said second fixed size; and

said exporter includes

a current packet register,

a last packet register, and

a combiner connected to said current packet register and said terminals, said combiner operable to

(a) store a current first information block in a current packet register,

(b) sequentially select groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number,

(c) store the current first information block in a last packet register,

(d) store a next first information block in the current packet register,

(e) select a group of the second fixed size bits from a set of bits remaining in the last packet register

and bits starting at a first bit of the current packet register, and

(f) thereafter repeat steps (b), (c), (d) and (e).

34. (Previously Presented) The data processing system of Claim 27, wherein:

said second fixed size is smaller in size than said first fixed size.

35. (Previously Presented) The data processing system of claim 34, wherein:

said first fixed size is an integral multiple of said second fixed size; and

said exporter includes

a current packet register, and

a combiner connected to said current packet register and said terminals, said combiner operable to

(a) store a current first information block in a current packet register,

(b) sequentially select groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a first bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until all bits of the current packet register are selected,

(c) thereafter store a next first information block in the current packet register and repeat steps (a), (b) and (c).

36. (Previously Presented) The data processing system of claim 34, wherein:

said first fixed size is not an integral multiple of said second fixed size; and

said exporter includes

a current packet register,

a last packet register, and

a combiner connected to said current packet register and

said terminals, said combiner operable to

(a) store a current first information block in a current packet register,

(b) sequentially select groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number,

(c) store the current first information block in a last packet register,

(d) store a next first information block in the current packet register,

(e) select a group of the second fixed size bits from a set of bits remaining in the last packet register and bits starting at a first bit of the current packet register, and

(f) thereafter repeat steps (b), (c), (d) and (e).

37. (Previously Presented) The method of Claim 2, wherein the transmission clock rate is greater than the data processor clock rate.

38. (Previously Presented) The method of Claim 1, wherein the second fixed size is larger in size than the first fixed size.

39. (Previously Presented) The method of Claim 38, wherein the transmission clock rate is less than the data processor clock rate.

40. (Previously Presented) The method of claim 31, wherein:

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks wherein

said step (b) of sequentially selecting a group of the second fixed size bits and said step (e) of selecting a group of second fixed size bits stall if there is no first information block stored in either said current packet register or in said last packet register.

41. (Previously Presented) The method of claim 31, wherein:

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks wherein

said step (a) of storing a current first information block in a current packet register and said step (d) of storing a next first information block in the current packet register stores NOP bits if no first information block is available,

said step (b) of sequentially selecting a group of the second fixed size bits and said step (e) of selecting a group of second fixed size bits selects a group of a second fixed size bits with a last valid first information block stored in said current packet register or in said last packet register and thereafter stalls if there is no first information block

stored in either said current packet register or in said last packet register.

42. (Previously Presented) The method of claim 31, wherein:

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks wherein

said step (a) of storing a current first information block in a current packet register and said step (d) of storing a next first information block in the current packet register stores NOP bits if no first information block is available,

said step (b) of sequentially selecting a group of the second fixed size bits and said step (e) of selecting a group of second fixed size bits selects a group of a second fixed size bits selects all NOP bits if there is no first information block stored in either said current packet register or in said last packet register.

43. (Previously Presented) The integrated circuit of Claim 17, wherein the transmission clock rate is greater than the data processor clock rate.

44. (Previously Presented) The integrated circuit of Claim 16, wherein said second fixed size is greater in size than said first fixed size.

45. (Previously Presented) The integrated circuit of Claim 44, wherein the transmission clock rate is less than the data processor clock rate.

46. (Previously Presented) The integrated circuit of claim 33, wherein:

said combiner is further operable to

not sequentially select groups of the second fixed size bits (b), not select a group of second fixed size bits (e) and stall if there is no first information block stored in either said current packet register or in said last packet register.

47. (Previously Presented) The integrated circuit of claim 33, wherein:

said combiner is further operable to

store NOP bits in a current packet register (a) and store NOP bits in the current packet register if no first information block is available,

sequentially select a group of the second fixed size bits (b) and select a group of second fixed size bits (e) by selecting a group of a second fixed size bits with a last valid first information block stored in said current packet register or in said last packet register and thereafter stalling if there is no first information block stored in either said current packet register or in said last packet register.

48. (Previously Presented) The integrated circuit of claim 33, wherein:

said combiner is further operable to

store NOP bits in a current packet register (a) and store NOP bits in the current packet register if no first information block is available,

sequentially select a group of the second fixed size bits (b) and select a group of second fixed size bits (e) by selecting all NOP bits if there is no first information block

stored in either said current packet register or in said last packet register.

49. (Previously Presented) The data processing system of Claim 34, wherein:

the transmission clock rate is greater than the data processor clock rate.

50. (Previously Presented) The data processing system of Claim 27, wherein:

said second fixed size is greater in size than said first fixed size.

51. (Previously Presented) The data processing system of Claim 50, wherein:

the transmission clock rate is less than the data processor clock rate.

52. (Previously Presented) The data processing system of claim 36, wherein:

said combiner is further operable to

not sequentially select groups of the second fixed size bits (b), not select a group of second fixed size bits (e) and stall if there is no first information block stored in either said current packet register or in said last packet register.

53. (Previously Presented) The data processing system of claim 36, wherein:

said combiner is further operable to

store NOP bits in a current packet register (a) and store NOP bits in the current packet register if no first information block is available,

sequentially select a group of the second fixed size bits (b) and select a group of second fixed size bits (e) by selecting a group of a second fixed size bits with a last valid first information block stored in said current packet register or stored in said last packet register and thereafter stalling if there is no first information block stored in either said current packet register or in said last packet register.

54. (Previously Presented) The data processing system of claim 36, wherein:

said combiner is further operable to

store NOP bits in a current packet register (a) and store NOP bits in the current packet register if no first information block is available,

sequentially select a group of the second fixed size bits (b) and select a group of second fixed size bits (e) by selecting all NOP bits if there is no first information block stored in either said current packet register or in said last packet register.